Physics and Modeling of FinFET and UTB-SOI MOSFETs
-- using BSIM-MG as example

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Outline

Introduction

FinFET and UTB Device Physics
- Short channel effects
- Quantum confinement
- Variability benefits
- Parasitic capacitance
- Mechanical strain and stressor design
- Self heating

FinFET and UTB Compact Models
CMOS Scaling Limits

- Short Channel Effects

**Capacitance Coupling Perspective**

- **Source/Channel Barrier**
- **Leakage Path**

**Barrier Lowering Perspective**

- Drain-induced barrier lowering (DIBL)

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Body Doping Limits

- Disadvantages of body doping
  - Random dopant fluctuation
  - Band-to-band tunneling leakage

D. Frank et. al. IEEE Proc., 2001
Solution #1: UTBSOI MOSFET

- Leakage path cut off by thin body
  - Ultra-thin-body (UTB) SOI MOSFET

\[ T_{ox} = 1.5 \text{nm}, \ N_{sub} = 1 \times 10^{15} \text{cm}^{-3}, \ V_{dd} = 1 \text{V}, \ V_{gs} = 0 \]
Solution #2: FinFET Transistor

**FinFET / Multiple-Gate Transistor:**

- Gate Control from Multiple Sides of the channel leads to smaller short channel effects

![Double-gate MOSFET Diagram](image)
FinFET: A Historical Perspective

- **1999 IEDM: 1st FinFET Demonstration**
  - DARPA project at UC Berkeley

- **2002: 25nm FinFET Demonstration**

- **2004: 5nm FinFET Demonstration**
  - Research at TSMC led by Dr. Hu

- **2011: FinFET used in production**
  - Intel 22nm Technology
BSIM-MG: Industry Standard Models

- BSIM-CMG for FinFET
  - “Common Multi-gate”
  - Model development 2005 -
  - Selected as industry standard compact model in 2012

- BSIM-IMG for UTB-SOI
  - “Independent Multi-gate”
  - Model development 2006 -
  - Selected as industry standard compact model in 2015
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FinFET and UTB Compact Models
Short Channel Effects (SCE)

- SCE Improves from Bulk to UTB-SOI / FinFET to GAA

Natural length $\lambda$ characterize SCE

\[ \lambda = \sqrt{\frac{\varepsilon_{si}}{2\varepsilon_{ox}} \left( 1 + \frac{\varepsilon_{ox} T_{fin}}{4\varepsilon_{si} T_{oxe}} \right) T_{fin} T_{oxe}} + \frac{1}{4H_{eff}^2} \]

\[ H_{eff} = \sqrt{\frac{H_{fin}}{8} \left( H_{fin} + 2 \frac{\varepsilon_{si}}{\varepsilon_{ox}} T_{oxe} \right)} \]

DIBL, SS $\propto \frac{0.5}{\cosh(D \cdot L_{eff} / \lambda) - 1}$

$\approx \exp \left( -D \frac{L_{eff}}{\lambda} \right)$
FDSOI

MATLAB

Decreasing $Tsi$

$Tsi=6\text{nm}$ to limit DIBL to $80\text{mV}$ at $Lg=20\text{nm}$

$\lambda = \sqrt{\frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{ox} t_{si}}$

[Graph showing the relationship between DIBL (mV/V) and gate length (nm) for different values of $Tsi$.]
FinFET

$Tsi = 12\text{nm}$

to limit DIBL to 80mV at $Lg = 20\text{nm}$

$\lambda = \sqrt{\frac{1}{2} \frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{ox} t_{si}}$

Decreasing $Tsi$
FinFET v.s. FDSOI

Tsi=6nm  FDSOI

Tsi=12nm  FinFET

Tsi=6nm  FDSOI

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SCE Benefits of Fin Recess

- Gate recess achieved by etching into BOX (SOI Fin)
- Significant SCE Improvement Shown

K. Cheng et al., VLSI 2014

D. Lu et al., S3S Conf. 2013
Punchthrough Stopper for Bulk Fin

Bulk FinFET  SOI FinFET

Terry Hook, IBM  

SiO2 not shown
FinFET with various shape are modeled

J. Pablo Duarte et al., “Unified FinFET Compact Model: Modeling Trapezoidal Triple-Gate FinFET”, SISPAD 2013
Body thickness ($T_{si}$) allows us to continue scaling of FinFETs

Tsi scaling limited by quantum effects

4nm wide Si fins
J Chang et al. VLSI 2011
2D Confinement Effects Need to be Considered for FinFET and UTB-SOI

\[ V_{g1} = V_{g2} = 0.7V \]
\[ \Psi_{m1} = \Psi_{m2} = 4.6eV \]
\[ N_{body} = 1e15cm^{-3} \]
Quantum Effects: Threshold Shift

- Electrons in FinFET Resembles “Particle in a BOX” Problem in quantum mechanics

\[ q\Delta V_{th} \approx E_0 = \frac{\hbar^2 \pi^2}{2m^* T_{Si}^2} \]

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Wikipedia
Inversion layer thickness effect
- Coxe ↓

Effective Oxide Thickness Model
- The effective charge thickness is a function of Qi

\[ T_{entrd} = \left( \frac{21\epsilon_S \hbar^2}{2qm_x Q_i} \right)^{1/3} \]

\[ C_{oxx} = \frac{\epsilon_{ox}}{T_{ox} + \frac{\epsilon_{ox}}{\epsilon_{si}} \Delta T_{ox-QM}} \]

(H. Lu et al., UCSD)
Fully Depleted Body: Low Variability

- Extremely low variability demonstrated for UTB-SOI with lightly-doped body

K. Cheng et al., IEDM 2009

ETSOI

Ref. [8]

This work

K. Cheng et al., IEDM 2009
6T SRAM Cells Fabricated with FinFET
Device variation modeled with BSIM-MG to capture SRAM SNM distribution

Variability Modeling using BSIM-MG

Measured Data
Monte Carlo

NF=1
189 cells
Mismatch:
\( \sigma_{\text{TFIN}} = 1.03 \text{ nm} \)
\( \sigma_{\text{LG}} = 4.2 \text{ nm} \)

NF=2
189 cells
Mismatch:
\( \sigma_{\text{TFIN}} = 1.03 \text{ nm} \)
\( \sigma_{\text{LG}} = 4.2 \text{ nm} \)

D. Lu et al., SISPAD 2009
FinFET Parasitic Capacitance

- Complex 3D structure need to be considered for fringe capacitance

![Diagram showing FinFET structure with labels for source, drain, gate, D_{pcca}, and F_{pitch}]

**D_{pcca} dependence**

![Graph showing Cgs0 (aF) vs Contact-Gate Distance (nm) with data points for TCAD and model, and a curve for Fin height dependence]

**Fin pitch dep.**

![Graph showing Cgs0 (aF) vs Fin Height (nm) for Fin Pitch 40nm (black squares), 50nm (red circles), and 60nm (blue triangles)]
Lattice Mismatch assumed:
- 1% smaller natural lattice constant

Longitudinal stress in channel
- +1.3 GPa (tensile)
- 37% $I_{d\text{lin}}$ Benefit

Possible Strain Sources:
- Carbon incorporation in channel
- SSDOI FinFET

Discussion
- C incorporation also suppresses P-diffusion
BSIM-MG Self Heating Sub-circuit

- **Self Heating Important for Bulk and SOI FinFETs**

  - $R_{th}$: normalized thermal resistance
  - $C_{th}$: normalized thermal capacitance
  - $W_{th0}$: minimum width for $R_{th}$ calculation
  - $F_{\text{pitch}}$: Fin-to-fin pitch
  - $N_{\text{fin}}$: Number of fins in total

  \[ R_{th} = \frac{R_{TH0}}{W_{TH0} + F_{\text{pitch}} \cdot N_{\text{fin}}} \]

  \[ C_{th} = C_{TH0} \cdot (W_{TH0} + F_{\text{pitch}} \cdot N_{\text{fin}}) \]

  ![Temperature Node](image)

  ![Bulk FinFET](image)

  *Takahasi et al., IEDM 2011*
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FinFET and UTB Compact Models
Framework for BSIM-MG

“Independent” Multi-Gate framework
(separate front- and back- gates)

Back-gated FDSOI

“Common” Multi-Gate framework
(tied gates)

BG FG S D

BSIM-IMG
BSIM-CMG

BSIM-CMG SOI module
BSIM-CMG bulk module
BSIM-CMG nanowire

FinFET with split gates

Vertical Pillar

SOI module
bulk module
nanowire

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Common Multi-gate Model: BSIM-CMG

TCAD Verification:

FinFET Silicon Data:

M. V. Dunga et al., VLSI 2007
Symbols: Electrical Test Data
Lines: Model

- L=120nm, D=80nm, Tox=3nm
- Asymmetric !!

Drain Current vs. $V_{gs}$

Transconductance

Output

Drain Current vs. $V_{ds}$

Summary

- **FinFET & UTB device physics essentially the same as planar, except**
  - Superior electrostatics, esp. with gate recess
  - Quantum effects ultimately limits $T_{si}$ scaling
  - 3D FinFET parasitic capacitance complex, but not necessarily larger
  - Strain further boost device performance

- **BSIM-CMG and BSIM-IMG are industry standard compact models**
  - Physically derived with good agreement with industry data
  - Variability model captures SRAM statistics
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